

Fig. 1

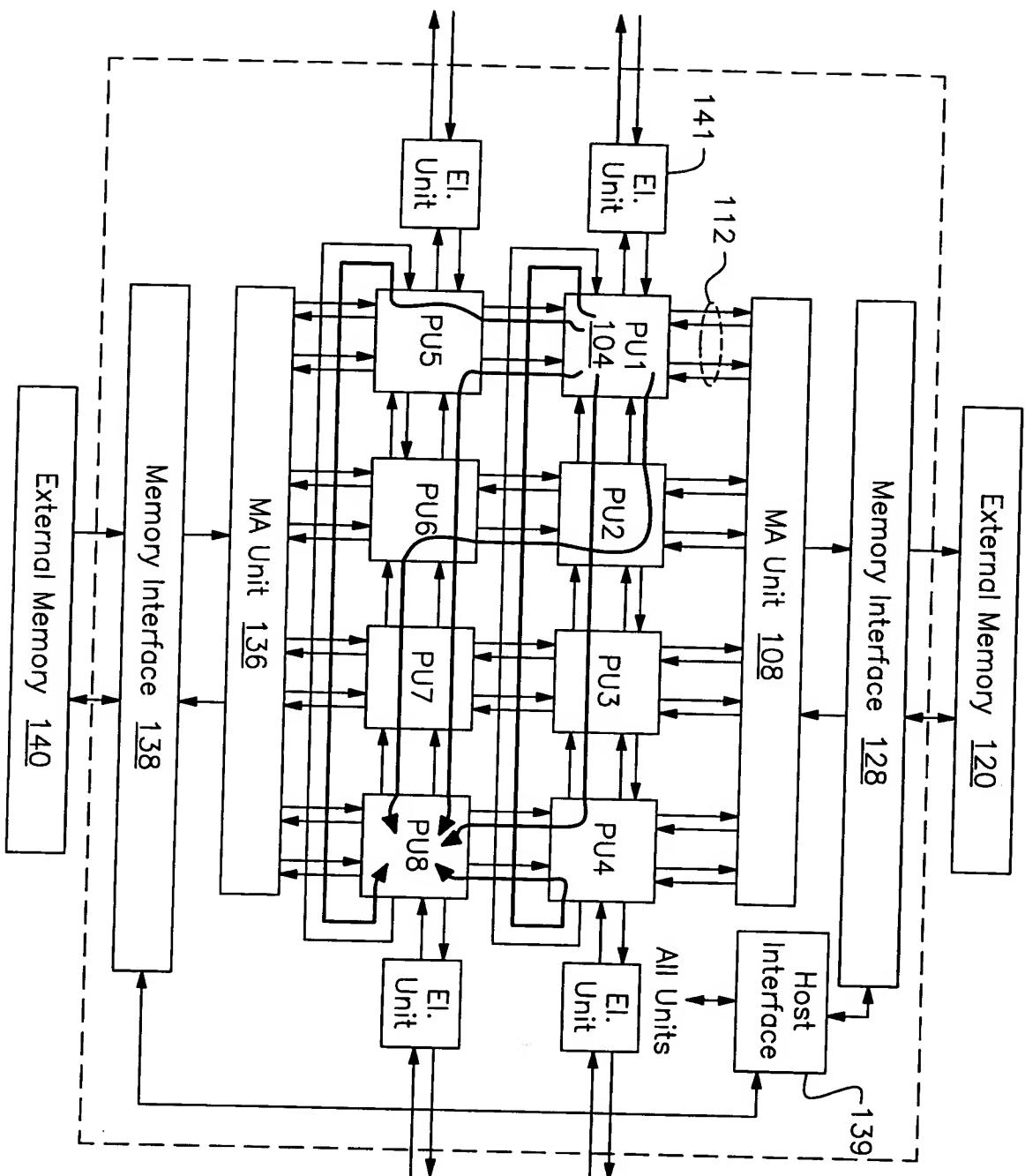


Fig. 2

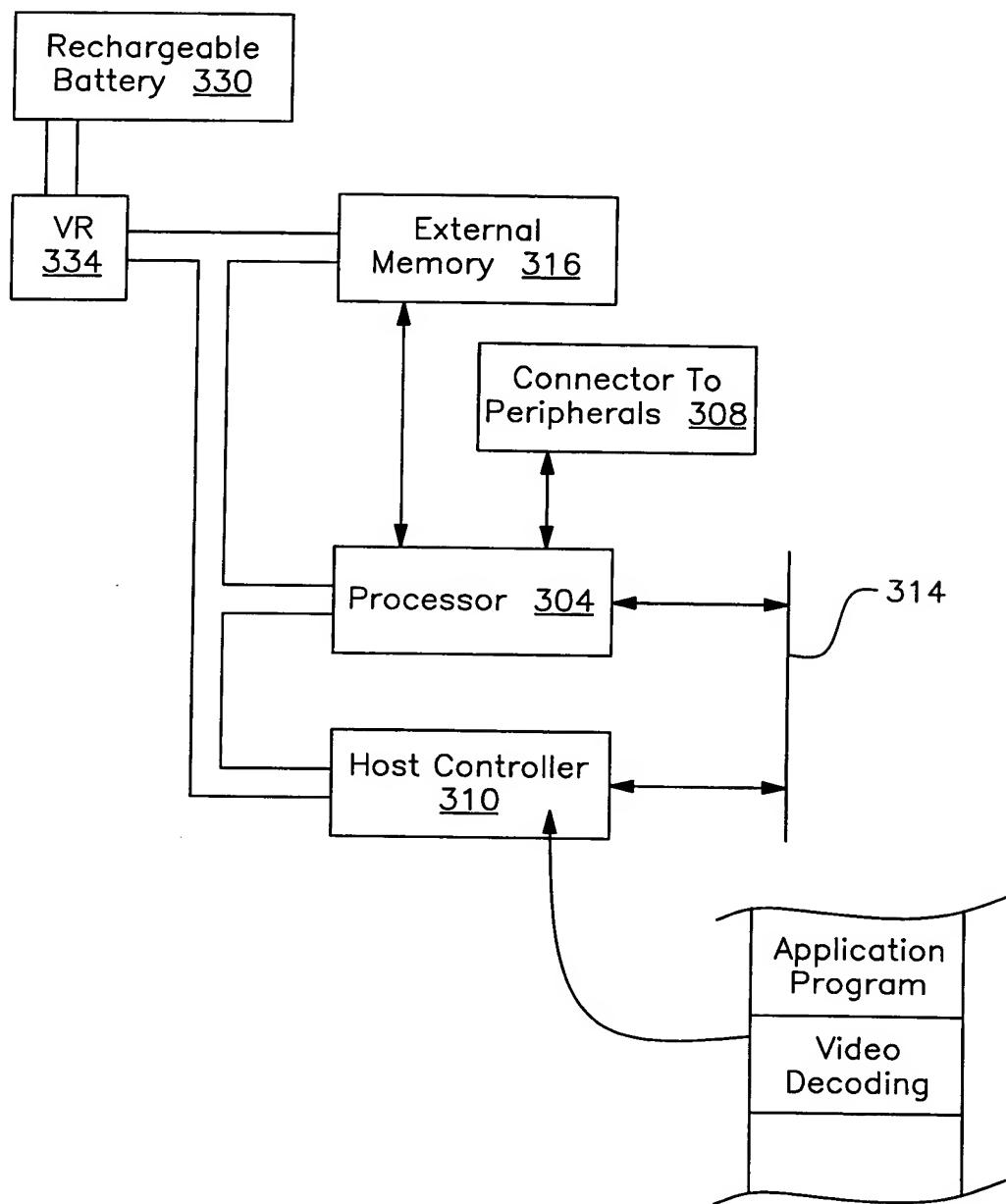
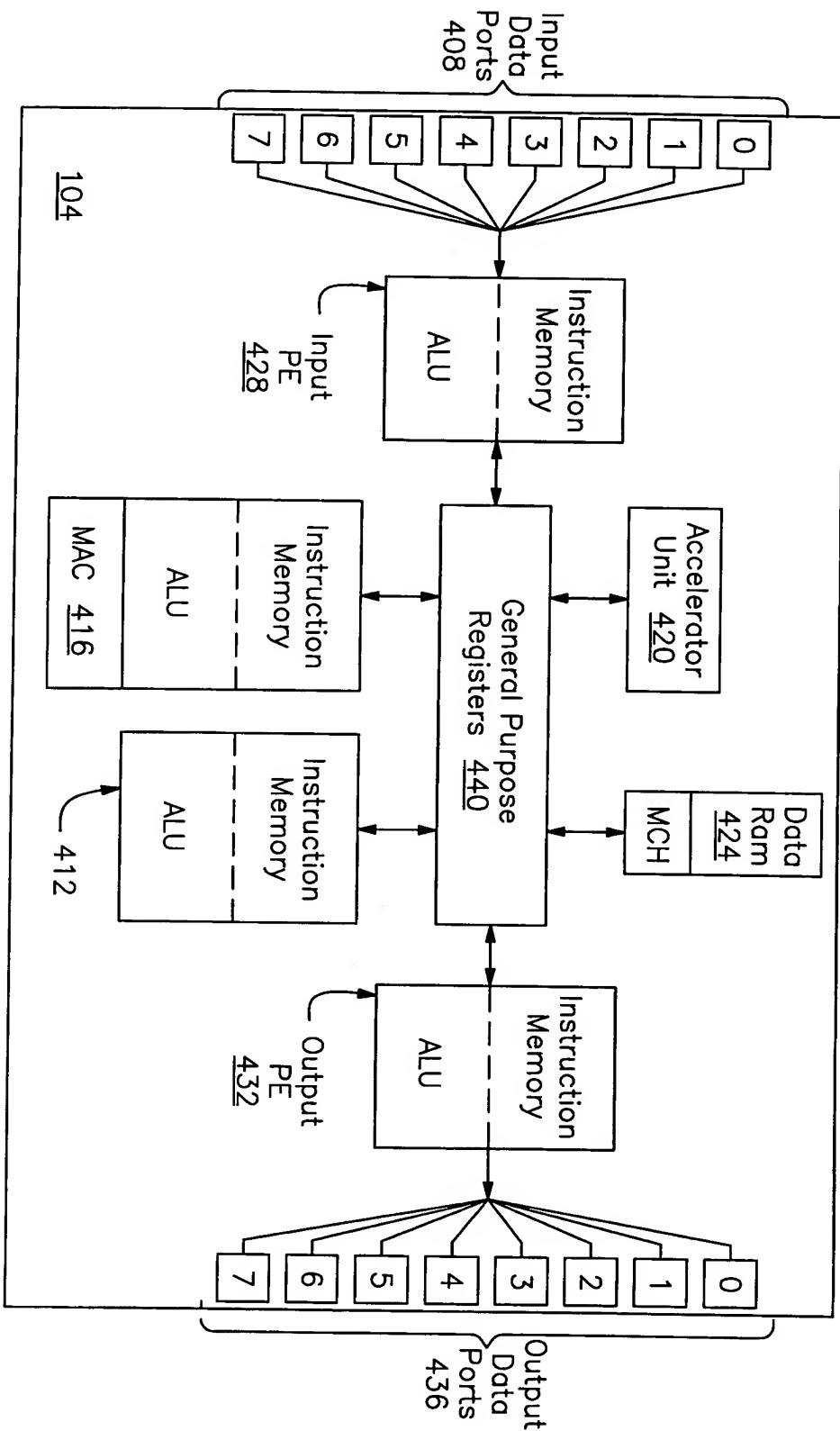


Fig. 3

Fig. 4



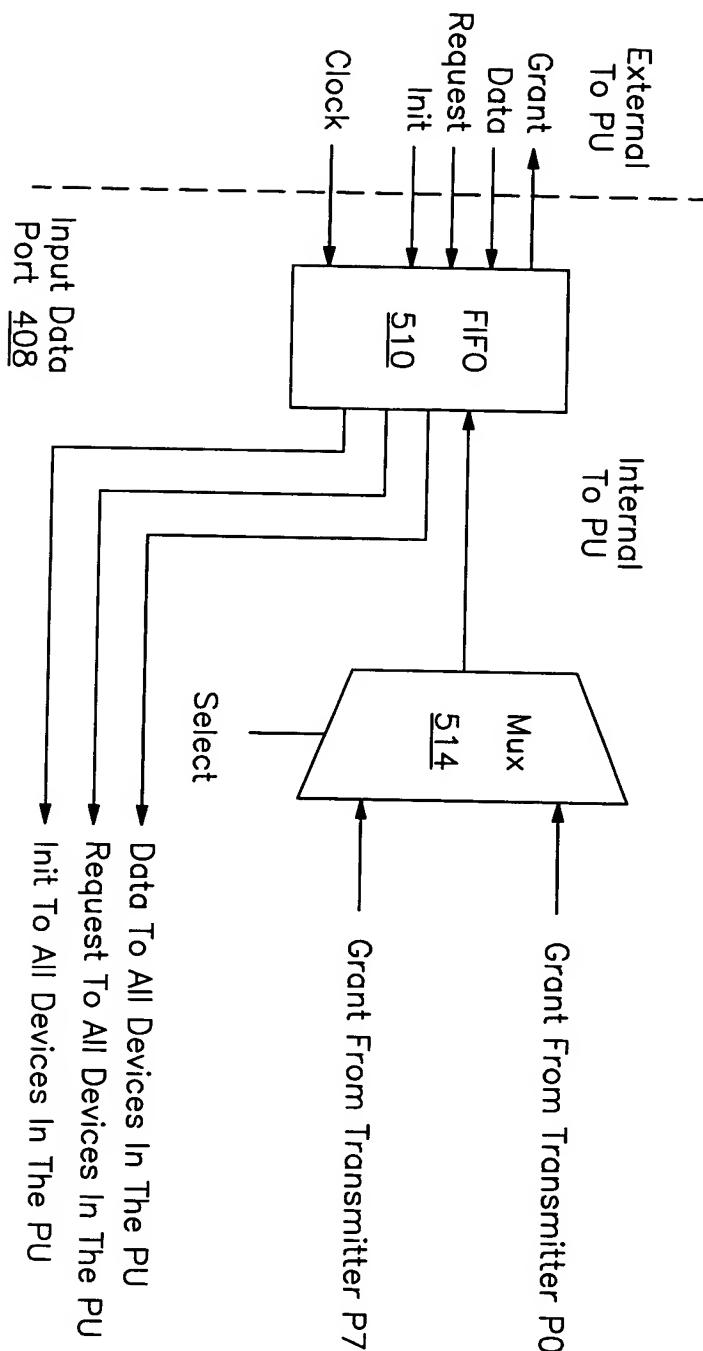


Fig. 5

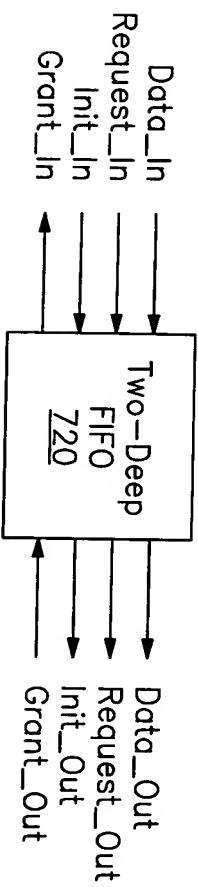


Fig. 6

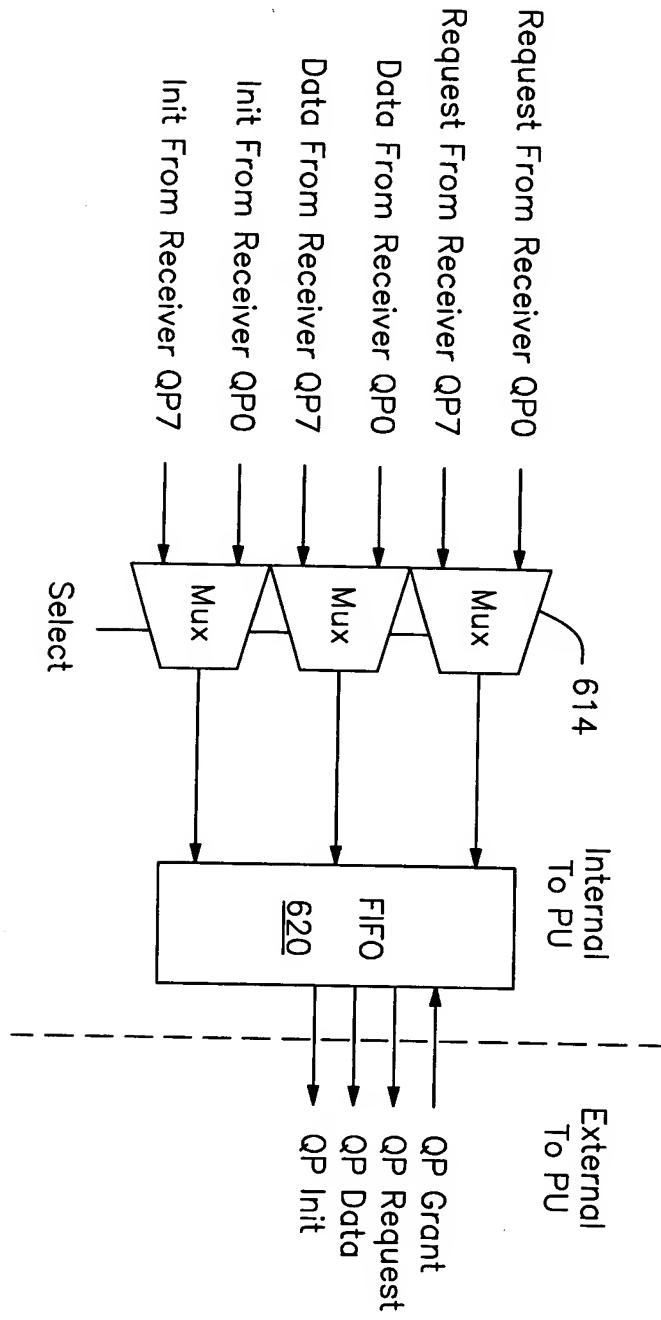


Fig. 7

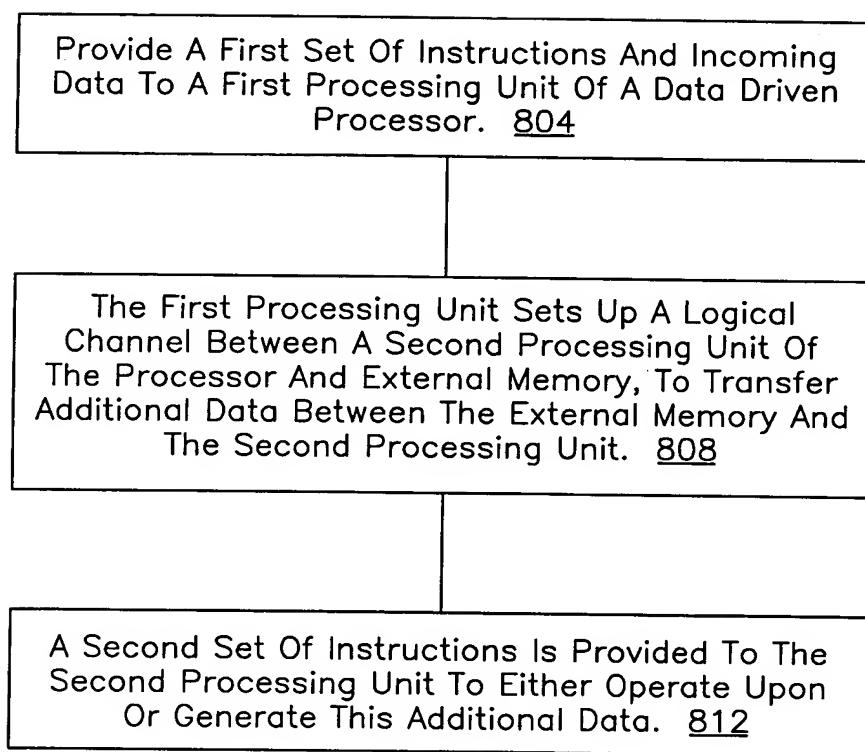
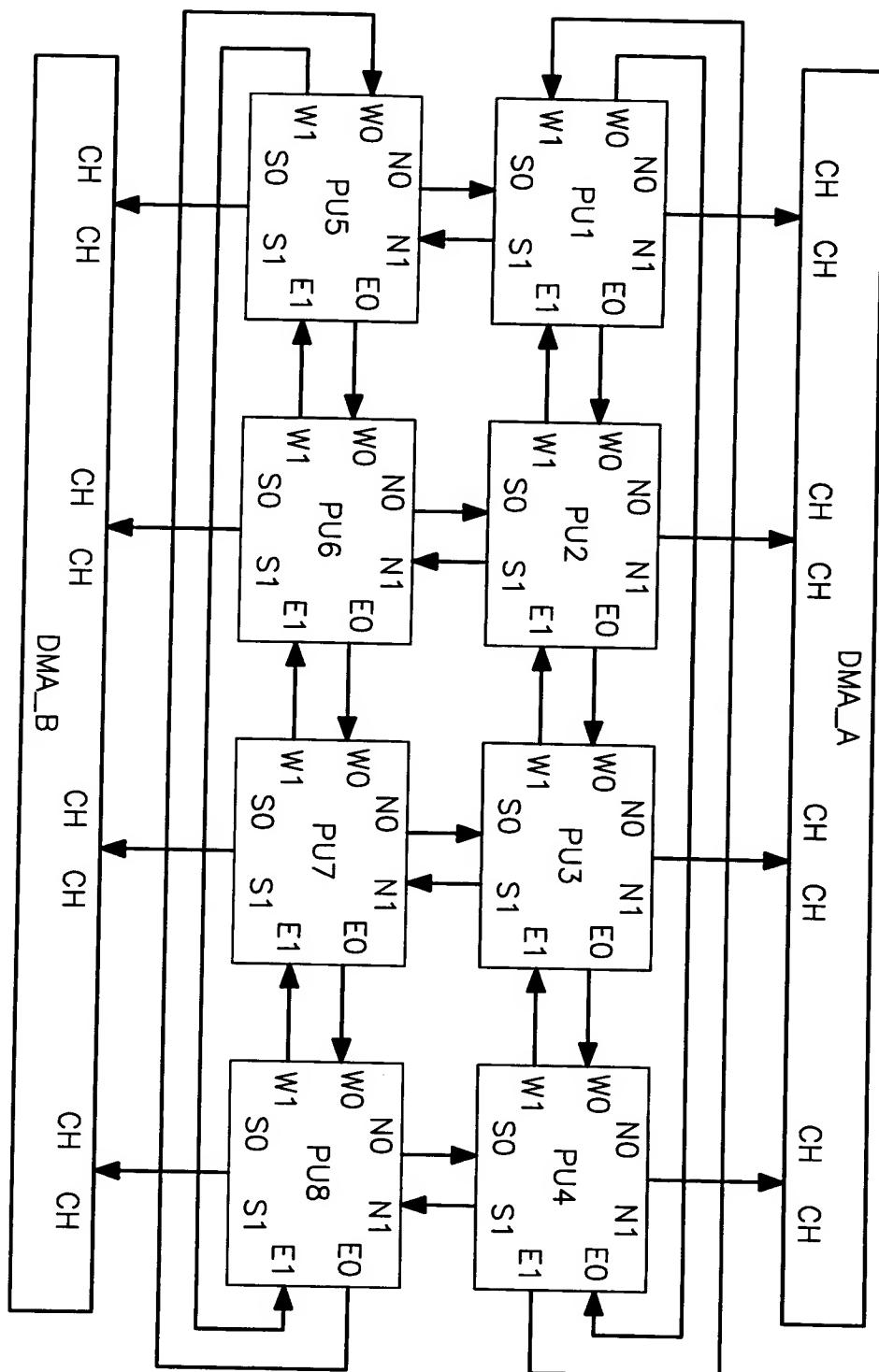


Fig. 8

Fig. 9



Blakely, Sokoloff, Taylor & Zafman LLP
 Title: CONTROLLING MEMORY ACCESS DEVICES IN A DATA
 DRIVEN ARCHITECTURE MESH ARRAY
 1st Named Inventor: Louis A. Lippincott
 Express Mail No.: EV339917539US
 Sheet: 8 of 11 (310) 207-3800
 Docket No.: 42P17013

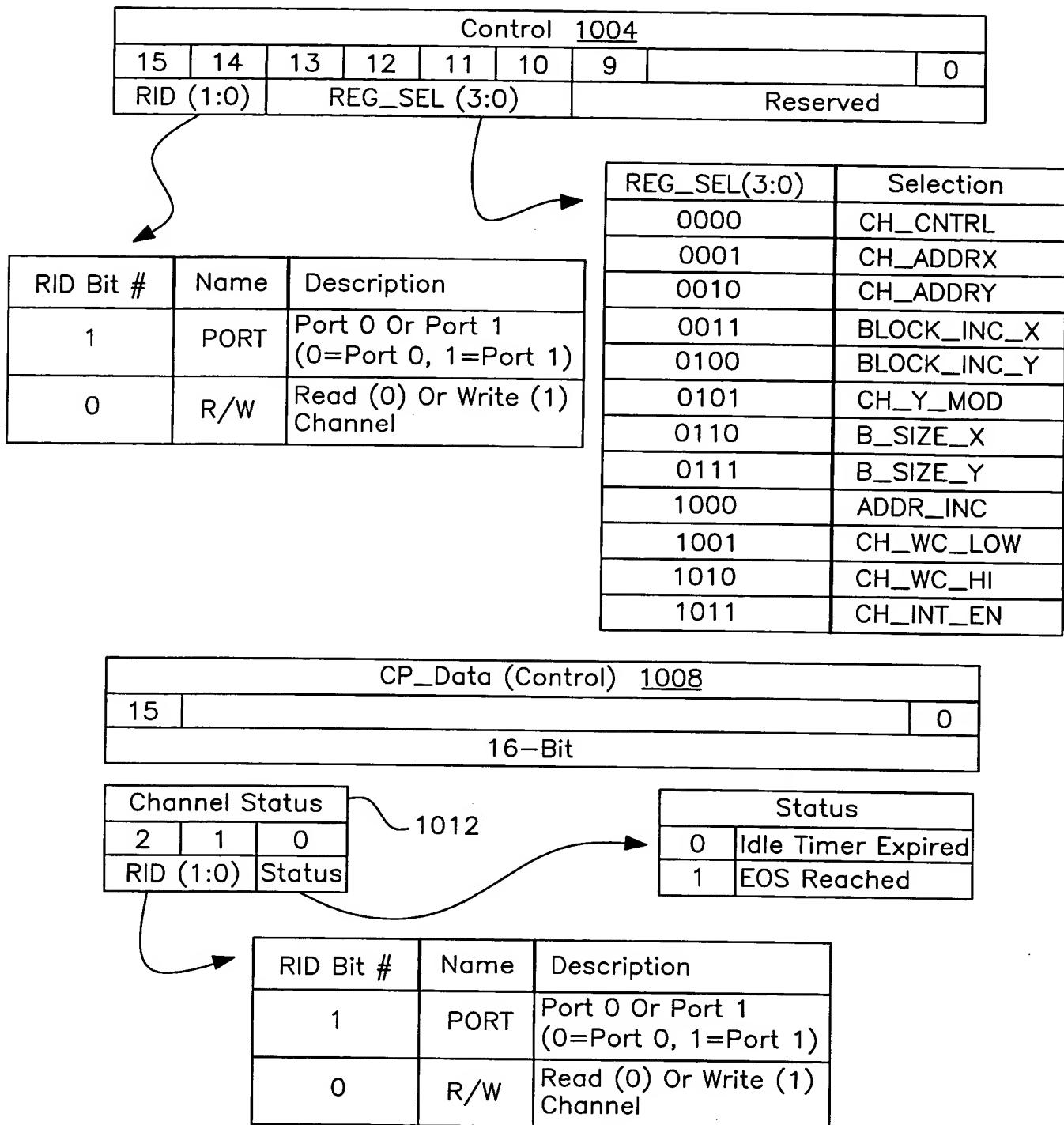
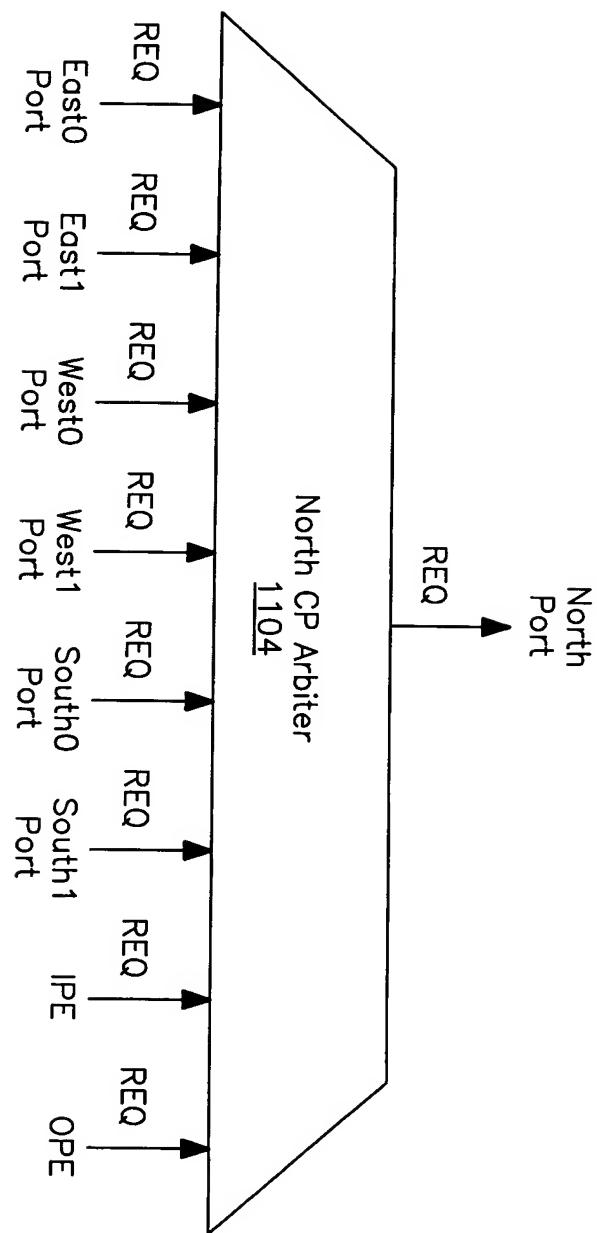


Fig. 10

Fig. 11



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Docket No.: 42P17013

Select Register For Control Port(CP) North0

Reset State: 0000 0000 0000 0000

RD Bit #	Name	Description/Purpose	Read/Write
15-10	Reserved	Reserved And Should Be Written As Zeros	Write
9-7	CP_R_SEL(n)	CP Receiver Select Bits	Read/Write
6-3	Reserved	Reserved And Should Be Written As Zeros	Write
2-0	CP_R_SEL(n)	CP Receiver Select Bits	Read/Write

Value	Selection	Description/Purpose
000	OPE	Command From OPE is Transmitted
001	East0	Command From East0 Port Is Transmitted
010	East1	Command From East1 Port Is Transmitted
011	South0	Command From South0 Port Is Transmitted
100	South1	Command From South1 Port Is Transmitted
101	West0	Command From West0 Port Is Transmitted
110	West1	Command From West1 Port Is Transmitted
111	IPE	Command From IPE Is Transmitted

Value	Selection	Description/Purpose
001	East0	East0 Port Receives Command
010	East1	East1 Port Receives Command
011	South0	South0 Port Receives Command
100	South1	South1 Port Receives Command
101	West0	West0 Port Receives Command
110	West1	West1 Port Receives Command

Fig. 12